Design of Area and Power Efficient Line Decoders for SRAM

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Abstract – Low power SRAM design is crucial since it takes an extensive part of aggregate power and die area in high performance processors. Optimization of SRAM (Static Random Access Memory) array design can be done at three domains namely bit cell optimization, sense amplifier optimization and decoder optimization. In this paper, decoder optimization in terms of area and power is done using GDI technique to implement in design of SRAM memory array. The proposed GDI 2-4 decoder and 4-16 decoders has been compared with CMOS and Mixed logic decoders. The proposed designs have been simulated in the 32nm CMOS technology using TANNER EDA tool. The simulations show that there is a noteworthy improvement in power delay product and area of the GDI designs, outflanking CMOS and Mixed logic designs in all cases.

Index Terms – Line decoder, SRAM, Mixed-Logic, GDI technique, Power-Delay Optimization.

1. INTRODUCTION

Low power electronics is particularly critical in the area of memory design. Since memory is one part found on practically every computerized framework that involves some processing no matter how small. Currently memories constitute a vast part of the chip area and if we can reduce the power utilization of memories, we will be able to influence a wide range of systems [1]. The expanding interest for low-power very large scale integration (VLSI) can be tended to at various outline levels, such as the architectural, circuit, layout, and the process innovation level. At the circuit configuration level, significant power savings could be done by means of proper decision of a logic style for actualizing combinational circuits. This is on the grounds that all the critical parameters overseeing power dissipation—switching capacitance, transition activity, and short-circuit currents— are unequivocally affected by the picked logic style[2]. Contingent upon the application, the sort of circuit to be executed, and the outline procedure utilized, distinctive execution perspectives wind up noticeably essential, denying the detailing of all inclusive principles for ideal logic styles.

CMOS: Initially working with CMOS was phenomenal since dissimilar to prior advances; there was practically insignificant static power dissipation. But as we keep on scaling down the technology and keep on shrinking the transistor sizes, inherent parasitic passive components have begun to surface and disturbed our harmony with standard CMOS logic style. As we keep on reducing both the supply voltage and threshold voltage of a MOSFET, sub threshold leakage will undoubtedly increment.

Pass Transistor Logic (PTL): There are two essential issues one is threshold drop across pass transistor brings about slower operations of circuits and other issue is that there will be direct static path for power dissipation because of PMOS device in the inverter circuit is not completely turned off [3].

Mixed Logic Design:

Mixed logic design is a combination of various logic styles in the same circuit, with an end goal to get enhanced performance compared to single-style outline. But this increases the complexity of the design [4].

Gate Diffusion Technique (GDI): GDI technique is a low power technique, which solves majority of issues mentioned above. The GDI approach permits implementation of an extensive variety of complex logic functions utilizing just two transistors. This strategy is appropriate for design of low-power circuits as it utilizes less number of transistors compared to CMOS and PTL logic , while enhancing logic level swing and the static power attributes and allowing simple top-down design by utilizing small cell library [5].

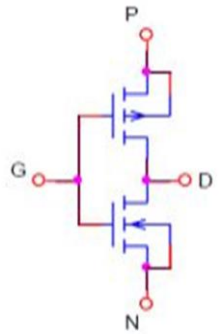

Fig 1: Basic GDI cell.

The GDI strategy is based on use of a simple cell as shown in Fig. 1. At first look, the circuit helps one to remember the standard CMOS inverter, however there are some essential contrasts.

The basic GDI cell comprises of three input terminals.

G, the terminal which is common gate input of NMOS and PMOS,

Input terminal P which is input to the source/drain of PMOS, and

N, the terminal which is input to the source/drain of NMOS.

The Substrates of both the NMOS and PMOS are connected to N or P terminals of the transistors respectively. So that it appears differently in relation to a CMOS inverter.

The fundamental functions of a GDI cell is as shown below in table 1:

Table 1: Basic Functions of a GDI cell.

N	P	G	OUTPUT	FUNCTION
0	1	A	A'	INVERTER
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

Section II provides a short review of the decoder circuits and their implementation using traditional CMOS and mixed logic circuitry. Section III provides proposed GDI decoder circuits and their application in SRAM memory arrays. Section IV provides the simulated waveforms and its results (power-delay calculations).Section V presents the final conclusions and future scope of the work presented.

2. OVERVIEW OF LINE DECODERS

In advanced frameworks, discrete amounts of data are spoken to by binary codes. A n-bit binary code can speak to up to 2^n particular components of coded information. A decoder is a combinational circuit that believers parallel data from n input lines to a greatest of 2^n exceptional yield lines or less, if the n-bit coded data has unused mixes. The circuits inspected in this work are called n-to-m line decoders, and their motivation is to create the $m = 2^n$ minterms of n input factors [4].

2.1. 2-4 Decoder

2.1.1. CMOS 2-4 Decoder:

A 2-4 line decoder creates the 4 minterms D0-3 of two input factors A and B. Its rationale operation is outlined in Table 2.

Table 2: Truth table of GDI 2-4 decoder

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Contingent upon the information mix, one of the 4 yields is chosen and set to 1 while the others are set to 0. In customary CMOS outline, NAND and NOR entryways are wanted to AND/OR potentially, since they can be actualized with 4 transistors, rather than 6, in this manner executing rationale capacities with higher effectiveness. A 2-4 decoder can be executed with 20 transistors utilizing 2 inverters and 4 NOR gates, as appeared in Fig.2.

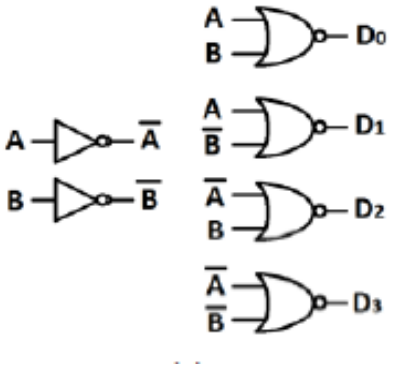

Fig 2: CMOS 2-4 Decoder.

2.1.2. 2-4 High-Performance Topology Decoder Using Mixed Logic:

The new decoder design is obtained by mixing three different types of logics (CMOS, TGL AND GATE & DVL AND GATE) into the same circuit that presents a significant improvement in delay while just slightly increasing power dissipation. As these decoders present both low power and low delay characteristics, achieving an overall good performance, it is named as 2-4 mixed logic HP (high performance) decoder [4].It comprises of 15 transistors (9 NMOS, 6 PMOS). The 2-4HP Schematic is shown in Fig.3.

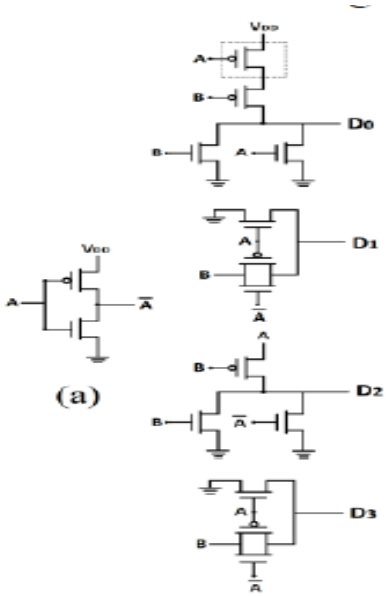

Fig 3: Mixed logic HP topology 2-4 decoder.

2.2. Integration in 4-16 Line Decoders

2.2.1. CMOS 4-16 decoder

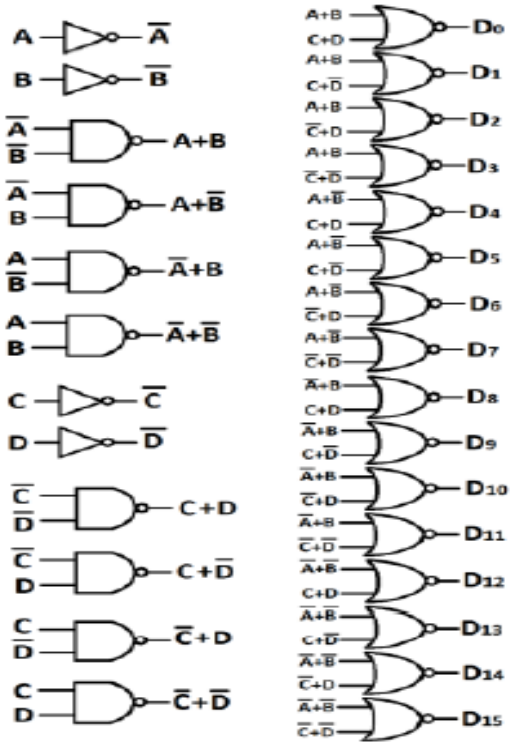

Fig 4: 4-16 CMOS decoder.

A 4-16 line decoder produces the 16 minterms D0-15 of 4 input factors A, B, C and D. A clear usage of these circuits would require 16 4-input NOR and NAND gates. Be that as it may, a more proficient plan can be acquired utilizing a predecoding procedure, as indicated by which squares of n address bits can be predecoded into 1-of-2n predecoded lines that fill in as contributions to the last stage decoder [4]. With this procedure, a 4-16 decoder can be executed with 2-4 transforming decoders and 16 2-input NOR gates (Fig. 4) In CMOS rationale, these outlines require 8 inverters and 24 4-input entryways, yielding an aggregate of 104 transistors each.

2.2.2 4-16 Mixed logic decoder:

The 4-16 decoder is implemented by utilizing the two 2-4 as predecoders in conjunction with CMOS NOR/NAND gates to deliver the decoded outputs. This design requires only 92 transistors compared to 104 transistors required in CMOS design as shown in fig.5. [4],[6]&[7].

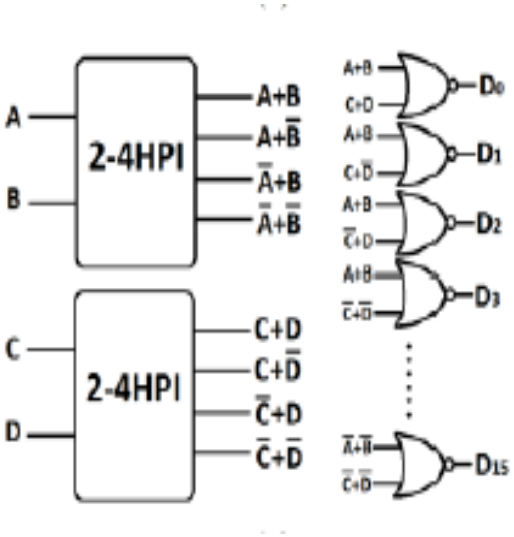

Fig 5: 4-16 mixed logic decoder.

3. PROPOSED SYSTEM

3.1. GDI 2-4 Decoder:

The AND gates in GDI technique requires just two transistors as shown in figure.

The GDI cell has three input terminals P, N & G. The input A is connected to the G terminal and the input B is connected to the N terminal and the P terminal is connected to the ground. This structure acts as a two inputs AND gate and is utilized in the design of the decoder. The Schematic of GDI 2-4 decoder is as shown in fig.6.

It utilizes 4 GDI AND gates and 2 inverters and it require an aggregate of 12 transistors to design the 2-4 decoder. Using this design, depending on the input combination one of the outputs is selected among the 2^m outputs as shown in figure 10.There is a decreased transistor count in GDI decoder compared to 20 transistors in CMOS and 15 transistors in mixed logic designs.

There is a reduction in power dissipation of the GDI circuits compared to CMOS and Mixed logic designs but there is a increase in delay yet the overall PDP of the GDI circuits has been reduced which improves the figure of merit.

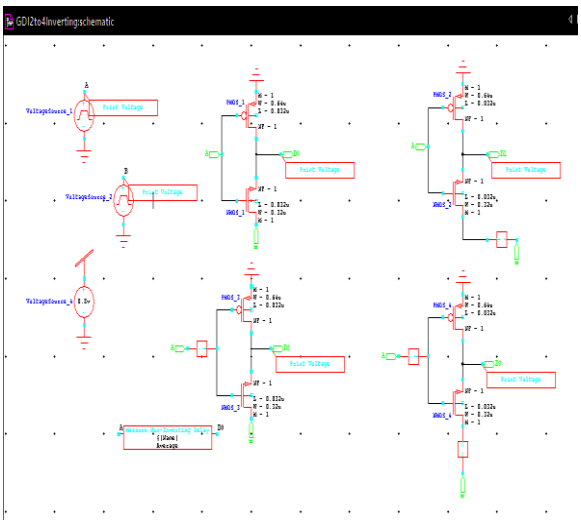

Fig 6: Schematic of GDI 2-4 decoder.

3.2. GDI 4-16 deeoder:

The GDI 4-16 decoder is designed utilizing two 2-4 GDI predecoders and a post decoder circuit. It requires a total of 52 transistors compared to 104 transistors in CMOS and 94 transistors in Mixed logic HP topology. The schematic of GDI 4-16 decoder is as shown in figure 7.

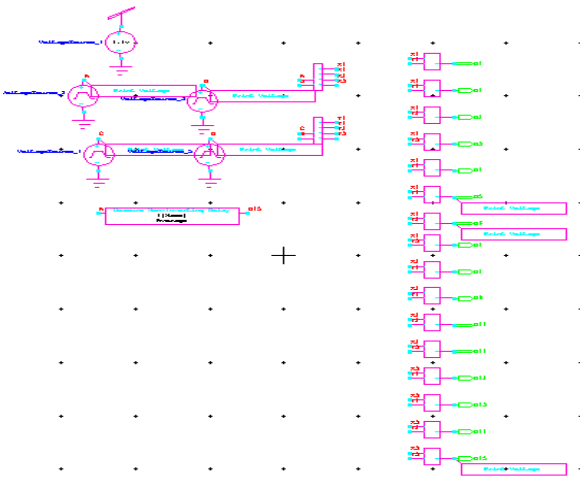

Fig 7: Schematic of GDI 4-16 decoder.

Using this design, depending on the input combination one of the output is selected among the $2^m=2^4=16$ outputs as shown in figure 11.Thus there is a decrease in transistor count ,and therby reduced complexity and power dissipation of the circuit.

4. APPLICATION OF PROPOSED GDI DECODERS IN SRAM MEMORY ARRAY

The proposed GDI decoder circuits are utilized as a part of SRAM memory arrays as shown in fig.8 & fig.9.The data or information stockpiling structure comprises of individual memory cells aligned in a variety of rows and columns.

Each cell can store 1-bit of binary data. In this array, there are 2^N word lines (horizontal rows) and 2^M bit lines (vertical columns).Thus in this structure there are total 2^N x 2^M number of individual memory cells. To access a specific memory cell in this structure the corresponding word line and corresponding bit line must be selected according to the address coming from the outside of the memory array. The row and column selection operation can be achieved by utilizing row and column decoders, respectively. One out of 2^N word lines can be selected as per *N*-bit row address using the row decoder while the column decoder circuit selects one out of 2^M bit-lines as per M-bit column address [8].

4.1. 4x4 SRAM Array:

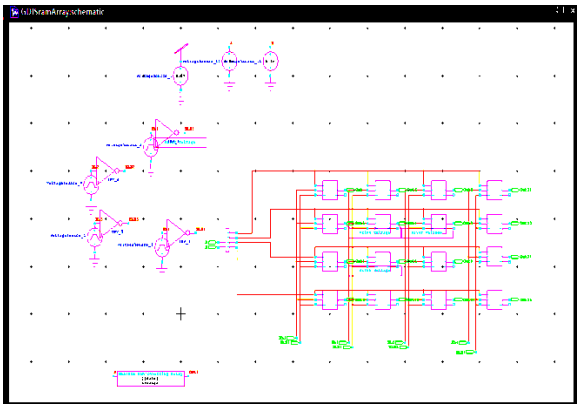

Fig 8: Schematic of 4*4 SRAM array using GDI 2-4 decoder.

4.2. 16x16 SRAM Array:

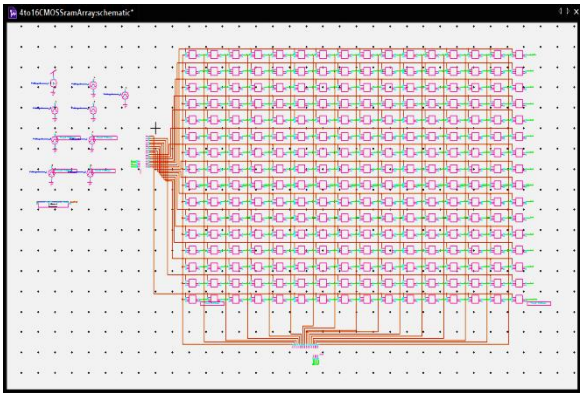

Fig 9: Schematic of 16*16 SRAM array using GDI 4-16 decoder.

5. SIMULATION RESULTS

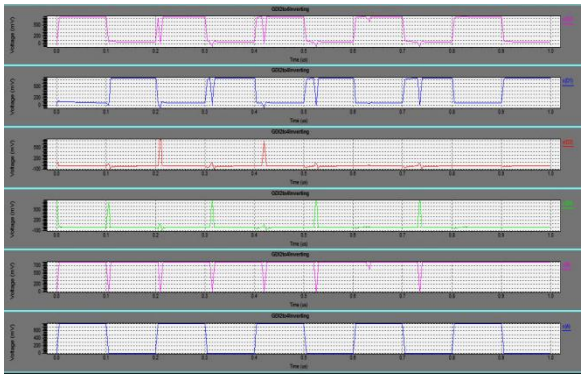

Fig 10: Waveform of GDI 2-4 decoder.

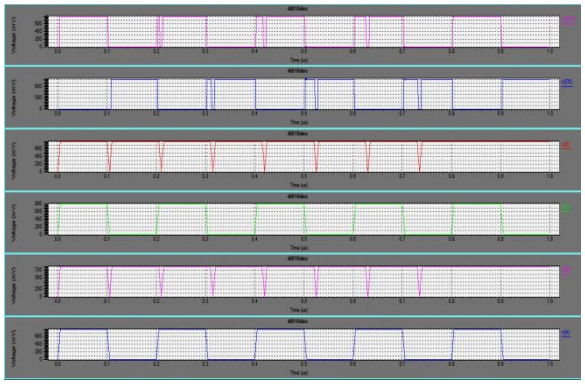

Fig 11: Waveform of GDI 4-16 decoder.

6. PERFORMANCE ANALYSIS

6.1. 2-4 Decoder:

Table 3:

Circuit	**No. of transistors**	**Power (µW)**	**Delay (ps)**	**PDP (ev)**
CMOS	20	2.97	114	2116
MIXED LOGIC	15	1.14	92	655
GDI	12	0.59	108	619

6.2. 4-16 Decoder:

Table 4:

Circuit	No. of transistors	Power (µW)	Delay (ps)	PDP (ev)
CMOS	104	11.19	286	20002
MIXED LOGIC	94	10.58	148	9786
GDI	56	2.84	379	6727

6.3. 4x4 SRAM ARRAY:

Table 5:

Circuit	No.of transis-tors	Power (mW)	Delay (ns)	PDP (Mev)	Area
CMOS	2220	2.30	52.9	747	2.58
MIXED LOGIC	2130	2.28	53.0	741	2.39
GDI	2100	0.87	53.3	289	2.33

6.4. 16x16 SRAM ARRAY:

Table 6:

Circuit	No.of transis-tors	Power (mW)	Delay (ns)	PDP (Mev)	Area
CMOS	32280	47.7	48.4	14310	11.05
MIXED LOGIC	32160	48.2	48.6	13560	10.08
GDI	31560	27.8	46.9	8166	9.58

7. CONCLUSION & FUTURE SCOPE

In this paper, the area and power efficient 2-4 and 4-16 line decoders using GDI technique are proposed. The proposed designs are further used in the implementation of 4x4 and 16x16 SRAM memory arrays. The proposed GDI decoders are compared with the CMOS and Mixed logic designs. There is a reduction in power dissipation of GDI circuits compared to CMOS and mixed logic designs. Even though there is an increase in delay of the GDI circuits, power delay product is

low compared to other designs which determine the figure of merit.

Considering the 4x4 SRAM array designed using GDI circuits, there is a 61.3% and 60.9% decrease in PDP of GDI circuits compared to CMOS and mixed logic designs.

Considering the 16x16 SRAM array designed using GDI circuits, there is a 41.7% and 38.4% decrease in PDP of GDI circuits compared to CMOS and mixed logic designs.

So the Figure of merit of GDI circuits is improved and they are area and power efficient. Thus GDI decoders can be used in portable electronic devices where low power and less area is required.

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